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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,433	03/12/2004	Soichi Homma	04329.3269	6546

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,433	HOMMA, SOICHI	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-24* is/are pending in the application.

4a) Of the above claim(s) *9-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 1030/2006 have been fully considered but they are not persuasive. The applicant argues that "Lin does not define the dielectric constant insulating film 29 to be a low dielectric constant insulating film." However, the Lin reference is not relied upon to teach the "low dielectric constant insulating film" of claim 1, but the physical arrangement of an insulating film on a surface with a passivation film formed on the insulating film. The "low dielectric constant insulating film" is taught by Capote, hence all of the limitations of claim 1 are taught by Capote and Lin. Additionally, the applicant argues that there is insufficient evidence for combing the cited references, in that forming an additional passivation on the passivation film of Capote would lessen the adhesion between the chip bonding layer 32 and the passivation layer. The Capote reference teaches that the chip bonding layer 32 has high adhesion to a passivation layer of silicon nitride, polyimide, or benzocyclobutene (Col 10 Ln 40-41). In the combination of Capote and Lin, the passivation layer 32 of Lin is in contact with the chip bonding layer 32 of Capote. Lin teaches a passivation layer 32 of silicon nitride (Col 8 Ln 51), a material disclosed in Capote as having high adhesion with chip bonding layer 32. Hence, the combination of Capote and Lin does not teach away from either invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Capote et al (U.S. Patent #6121689), in view of Lin (U.S. Patent #6426556).

With respect to **claim 1**, Capote teaches a semiconductor chip having a semiconductor element or an integrated circuit formed in the semiconductor chip (Fig. 15, 10), a low dielectric constant insulating film having a relative dielectric constant of about 3.5 or less formed directly on a surface of the dielectric chip (Col 10 Ln 40-41; benzocyclobutene, which is disclosed in the specification of this application to be a suitable material. It is inherent that benzocyclobutene has a dielectric constant of about 3.5 or less); a plurality of bump electrodes (Fig. 15, 14) provided on a surface of the insulating, a wiring board (Fig. 15, 20) having a plurality of connecting electrodes being electrically connected to the bump electrodes (Fig. 15, 12); and a resin molding filled in a space between the semiconductor chip and the wiring, the electrically connected bump electrodes and the connecting electrodes being arranged in the space (Fig. 15, 22), wherein the resin molding is formed a resin having a flux function and changed from liquid to solid when the bump electrodes are in a molten state (Col 4 Ln 14-24). Capote does not teach a low dielectric constant insulating film formed on a surface of the semiconductor chip, and additionally a passivation film formed on

a surface of the low dielectric constant insulating film. Lin teaches a dielectric insulating film on a semiconductor surface (Fig. 15, 29), a passivation film formed on the insulating film (Fig. 15, 32), and that the passivation film can comprise multiple layers (Col 6 Ln 31-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an additional passivation film on the film of Capote as taught by Lin in order to provide additional surface protection for the chip.

With respect to **claim 3**, Capote teaches a low dielectric constant insulating film benzocyclobutene, which is disclosed in the specification of this application to be a suitable material. It is inherent that benzocyclobutene has an adhesion strength of 15 J/m^s or less.

With respect to **claim 5**, Capote teaches that the resin has a coefficient of elasticity of greater than 20 MPa at normal temperature (Col 10 Ln 56-57).

With respect to **claim 6**, Capote teaches a resin molding comprising a first resin layer close to the semiconductor chip (Fig. 13, 37) and a second resin layer close to the wiring board (Fig. 13, 39), and the second resin layer is a resin layer which does not contain a filler (Col 9 Ln 31-32).

With respect to **claim 7**, Capote teaches a resin molding comprising a first resin layer close to the semiconductor chip (Fig. 15, 32), a second resin layer close to the wiring board (Fig. 15, 34), and a third resin layer interposed between the first resin layer and the second resin layer (Fig. 15, 22), and the third resin

layer is a resin layer which does not contain filler (Col 9 Ln 55-56, portion 39 contains no filler).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Capote and Lin, in view of Mistry et al (U.S. Patent #6077726).

With respect to **claim 8**, Capote and Lin teach all of the limitations of claim 1, and furthermore Capote teaches that the bump electrodes of the semiconductor chip are electrically connected to a plurality of connecting electrodes formed on the semiconductor chip (Fig. 4, 24), but does not teach that a part of the connecting electrodes are coated with a passivation film comprising at least one layer formed of an organic film. Mistry teaches a passivation film comprising at least one layer formed of an organic film coating a connecting electrode (Fig. 1, 16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Capote with a passivation layer of organic material as taught by Mistry in order to reduce stress in the package.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Capote et al (U.S. Patent #6121689), in view of Lin (U.S. Patent #6426556), further in view of Grill et al (U.S. PG Pub #2002/0127844).

With respect to **claim 21**, Capote teaches a semiconductor chip in which a semiconductor element or an integrated circuit is formed (Fig. 15, 10); a passivation film formed on the chip (Col 10 Ln 40-41), a pad (Fig. 3, 24); and a

bump electrode formed on the pad through the barrier film (Fig. 15, 14); but does not teach a low K dielectric film formed on the semiconductor chip, the low K dielectric film having a wiring film formed therein; or a barrier film formed on the pad. Grill teaches chip having a low-K dielectric film (Fig. 3, 310) and wiring film formed thereon (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide low-K insulating films on the chip of Capote in order to reduce signal propagation delays in the device. Lin teaches a barrier film formed on a pad (Fig. 15, 33 and Col 11 Ln 5-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a barrier layer on the pad of Capote in order to prevent oxidation.

With respect to **claim 22**, Capote teaches a wiring board (Fig. 15, 20) having a plurality of connecting electrodes being electrically connected to the bump electrodes (Fig. 15, 12); and a resin molding filled in a space between the semiconductor chip and the wiring, the electrically connected bump electrodes and the connecting electrodes being arranged in the space (Fig. 15, 22), wherein the resin molding is formed a resin having a flux function and changed from liquid to solid when the bump electrodes are in a molten state (Col 4 Ln 14-24).

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Capote et al (U.S. Patent #6121689), in view of Kelkar et al (U.S. Patent #6462426), further in view of Grill et al (U.S. PG Pub #2002/0127844).

With respect to **claim 23**, Capote teaches a semiconductor chip in which a semiconductor element or an integrated circuit is formed (Fig. 15, 10); a passivation film formed on the chip (Col 10 Ln 40-41), a pad (Fig. 3, 24); and a bump electrode formed on the pad through the barrier film (Fig. 15, 14); but does not teach a low K dielectric film formed on the semiconductor chip, the low K dielectric film having a wiring film formed therein; a plurality of passivation films, each of the passivation films having a pad of a different material formed therein; or a barrier film formed on the pad. Grill teaches chip having a plurality low-K dielectric films (Fig. 3, 310) and wiring film formed thereon (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide low-K insulating films on the chip of Capote in order to reduce signal propagation delays in the device.

Kelkar teaches a plurality of passivation layers having a pad of different material formed therein (Fig. 2, passivation films 206 and 210, pads 204 and 202, materials Col 4 Ln 64-66 and Col 6 Ln 11-13, the materials are distinguished from another by being formed separately and by the difference in shading in the drawings); and a barrier film formed in the uppermost passivation film (Fig. 2, 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a plurality of passivation films and pads on the device of Capote as taught by Kelkar in order to prevent cracks from propagating through the package (Col 4 Ln 36); and to provide a barrier film on the device of

Capote as taught by Kelkar in order to provide a contact area for the solder bump. Furthermore, it would have been obvious to one of ordinary skill in the art to select different material for the pads 202 and 204, such as copper and aluminum, since different material were disclosed by Kelkar. See MPEP 2144.06; an express suggestion to substitute one equivalent component or process for another is not necessary to render such substitution obvious. *In re Fout*, 675 F.2d 297, 213 USPQ 532 (CCPA 1982).

With respect to **claim 24**, Capote teaches a wiring board (Fig. 15, 20) having a plurality of connecting electrodes being electrically connected to the bump electrodes (Fig. 15, 12); and a resin molding filled in a space between the semiconductor chip and the wiring, the electrically connected bump electrodes and the connecting electrodes being arranged in the space (Fig. 15, 22), wherein the resin molding is formed a resin having a flux function and changed from liquid to solid when the bump electrodes are in a molten state (Col 4 Ln 14-24).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

EVAN PERT
PRIMARY EXAMINER